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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,015	04/16/2004	Youn Seon Jang	5895P059	9235

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EXAMINER	
GARCIA, LUIS	
ART UNIT	PAPER NUMBER
2613	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,015	JANG ET AL.	
	Examiner	Art Unit	
	Luis F. Garcia	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-9* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-4 and 7-8 are rejected** under 35 U.S.C. 102(b) as being anticipated by King (US 6,473,219).

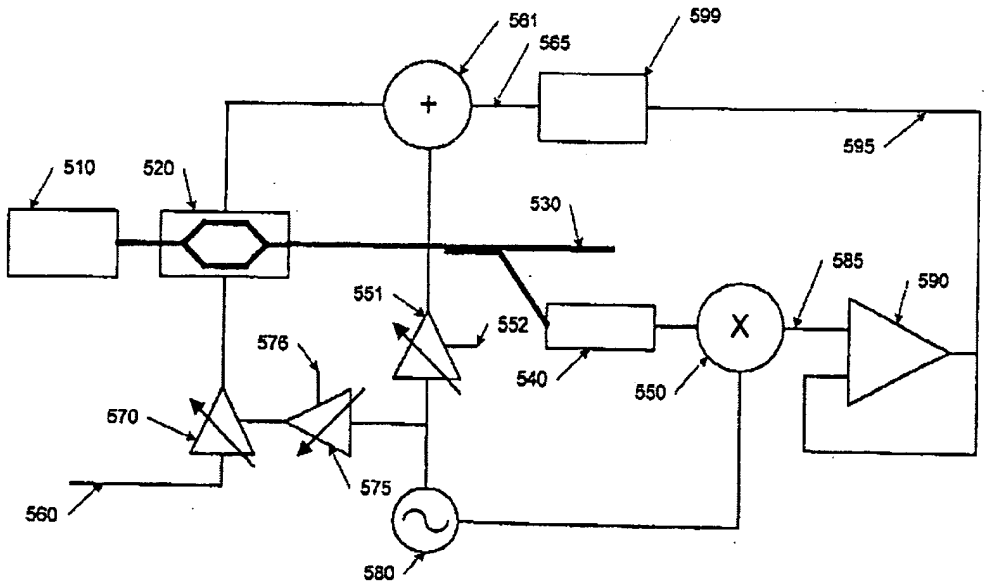


Figure 5

Regarding claim 1, King discloses an apparatus for stabilizing a bias voltage for an external modulator used for pulse generation **(FIG. 5 and col3 ln42-60, col4 ln36-43)**, comprising:

optical dividing means for allowing an optical signal output from the external modulator, to which the bias voltage is to be applied, to branch off **(FIG. 5 (input to 540-photo-detector) in which the optical signal from the modulator is branch off into PD-540)**;

optical/electrical converting means for converting the output optical signal branched by the optical dividing means into an electrical signal **(FIG. 5 (540-photo-detector) in which the O/E converter (PD-540) converts the output optical signal branched by the diving means into an electrical signal)**;

multiplying means for multiplying the optical signal, output from the external modulator and applied through the optical/electrical converting means, by a drive clock signal applied to the external modulator **(FIG. 5 (550-multiplier) in which the multiplier multiplies the optical signal, output via O/E converter, by a drive clock signal (580-tone generator) which is also applied to the modulator via element-561)**;

mean output measuring means for measuring a mean output value of products obtained by multiplication of an output signal of the external modulator and the clock signal **(FIG. 5 (590-integrator) in which the integrator (mean output measuring means) measures the mean output value of the multiplier (e.g. products obtained by multiplying the output signal from the modulator and the tone generator (clock)))**; and

control means for detecting an optimal bias point of the external modulator on the basis of the mean output value of the products obtained by the multiplication, which is

output from the mean output measuring means, and maintaining an optimal bias voltage corresponding to the optimal bias point **(FIG. 5 (599-Bias Voltage Generator) and col5 ln6-9 in which the bias voltage generator detects the optimal bias point output from the integrator (mean output measuring means) and generates an appropriate bias signal in order to maintain an optimal bias voltage)**.

Regarding claim 2, King discloses the bias voltage stabilizing apparatus according to claim 1 as applied above.

King further discloses wherein the control means sets a bias point, obtained when the mean output value from the mean output measuring means is "0", to the optimal bias point **(FIG. 5 (599-Bias Voltage Generator) col5 ln6-9 in which the bias voltage generator (control means) sets the bias point when the mean output form the integrator is "0" (error signal is minimal), e.g. constantly outputs a bias voltage based on the error signal)**.

Regarding claims 3 and 7, King discloses the bias voltage stabilizing apparatus according to claim 1 as applied above.

King further discloses wherein the control means is operated so that, the control means **(FIG. 5 (599-Bias Voltage Generator))** increases the bias voltage applied to the external modulator by ΔV, when the mean output value from the mean output measuring means is a positive (+) value **(FIG. 5 (590-integrator) when the integrator error signal (voltage) is added to the tone generator voltage signal; therefore, when the output of the integrator is positive the bias voltage will increase)**, while the control means decreases the bias voltage by ΔV when the mean output value is a

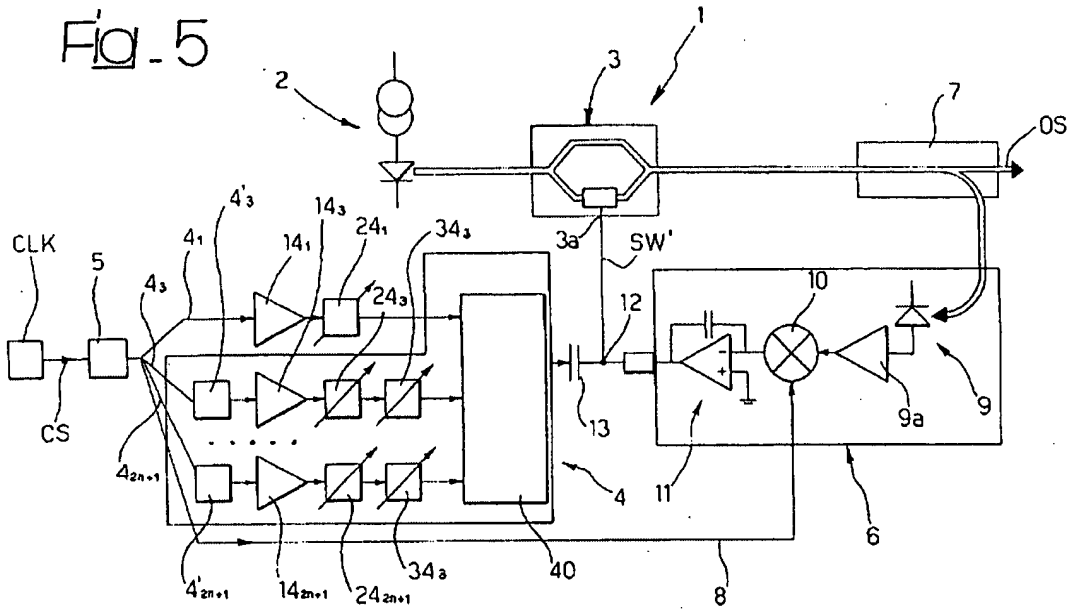
negative (-) value, thus maintaining the optimal bias voltage **(FIG. 5 (590-integrator) in which the integrator error signal (voltage) is added to the tone generator voltage signal; therefore, when the output of the integrator is negative the bias voltage will decrease)**.

King does not expressly disclose if the external modulator is a pulse generating modulator for Return-to-Zero (RZ) modulation using Non-Return-to-Zero (NRZ) data. However, it is a matter of design choice as to what modulation scheme to implement in King's system. For NRZ, CSRZ and RZ modulation schemes are well known in the art and within the scope of King's invention (e.g. electrical data input FIG. 5 (560-Electrical Data signal) can be an NRZ/CSRZ data signal).

Regarding claims 4 and 8, rejected as stated in claim 3 rejection in which King further discloses in col3 ln65-67 to col4 ln1-17 that the biasing scheme can be inversed, e.g. col4 ln7-9: when the amplitude of the data signal is increases, the bias voltage is increased and col3 ln50-52: in "inverse mode", when the amplitude of the data signal increases, the bias voltage is decreased; therefore, inverting the biasing scheme of claim 3 is within the scope of King's invention.

2. **Claims 1-2 are rejected** under 35 U.S.C. 102(e) as being anticipated by Puleo (US 6,778,310).

Fig. 5



Regarding claim 1, Puleo discloses an apparatus for stabilizing a bias voltage for an external modulator used for pulse generation **(col2 ln51-56 and col3 ln64-67 to col4 ln1-10)**, comprising:

optical dividing means for allowing an optical signal output from the external modulator, to which the bias voltage is to be applied, to branch off **(FIG. 5 (7-optical coupler) in which the optical coupler (optical dividing means) divides the optical output signal from modulator (3))**;

optical/electrical converting means for converting the output optical signal branched by the optical dividing means into an electrical signal **(FIG. 5 (9-photo detector) in which the photo detector (optical/electrical converting means) converts the optical signal from optical dividing means (e.g. optical coupler) into an electrical signal)**;

multiplying means for multiplying the optical signal, output from the external modulator and applied through the optical/electrical converting means, by a drive clock signal applied to the external modulator **(FIG. 5 (10-multiplier node) in which the multiplier node (multiplying means) multiplies the signal from O/E converting means (e.g. from PD-9) with a drive clock signal applied to the modulator, e.g. CLK is divided an applied to the multiplier node via path-8 and to the modulator via RF combiner-40)**;

mean output measuring means for measuring a mean output value of products obtained by multiplication of an output signal of the external modulator and the clock signal **(FIG. 5 (11-integrator) in which the integrator (mean output measuring means) measures the mean output value of the multiplier node (e.g. products obtained by multiplying the output signal from the modulator via optical coupler-7 and the clock-CLK))**; and

control means for detecting an optimal bias point of the external modulator on the basis of the mean output value of the products obtained by the multiplication, which is output from the mean output measuring means, and maintaining an optimal bias voltage corresponding to the optimal bias point **(FIG. 5 (6-Bias Control Circuit, 12-combing node, 3a-modulation port) and col3 ln64-67 to col4 ln1-2 in which the combining node detects the bias point output from the mean output measuring means (11-integrator) and produces the proper bias level for the driving signal, e.g. maintains an optimal bias voltage)**.

Regarding claim 2, Puleo discloses the bias voltage stabilizing apparatus according to claim 1 as applied above.

Puleo further discloses wherein the control means sets a bias point, obtained when the mean output value from the mean output measuring means is "0", to the optimal bias point **(FIG. 5 (599-Bias Voltage Generator) col5 ln6-9 in which the bias voltage generator (control means) sets the bias point when the mean output form the integrator is "0" (error signal is minimal), e.g. constantly outputs a bias voltage based on the error signal)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claim 5 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Puleo.

Regarding claim 5, rejected as stated in claim 1 rejection in which it would have been obvious to one of ordinary skill in the art at the time of invention that the process will keep repeating as long as the transmitter is in use, e.g. input electrical clock signal at FIG. 5 (CLK)) causes the process to start.

4. **Claims 5 and 9 are rejected** under 35 U.S.C. 103(a) as being unpatentable over King.

Regarding claim 5, rejected as stated in claim 1 rejection in which it would have been obvious to one of ordinary skill in the art at the time of invention that the process will keep repeating as long as the transmitter is in use, e.g. input electrical data at the input (FIG. 5 (560)) causes the process to start.

Regarding claim 9, rejected as stated in claim 5 in which it would have been obvious to one of ordinary skill in the art that the process (algorithm) of bias stabilization is performed by a computer readable recording medium for storing a computer program implemented to perform the steps of claim 5, e.g. King notes in col3 ln57-61/col4 ln14-17 that the use of algorithms for bias generations is well known in the art; thereby, making the implementation of such algorithms/computer programs on a computer readable medium obvious to one of ordinary skill in the art.

Allowable Subject Matter

5. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis F. Garcia whose telephone number is (571)272-7975. The examiner can normally be reached on 8-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken N. Vanderpuye can be reached on (571)272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LG

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER